Remarks

Claims 30, 32-34, 40-45 and 50-52 are pending in the present application. Claim 53 has been added, and claims 30, 32-34, 40-45 and 50-52 are amended herein to correct certain typographical errors and to change the term "the" to --said-- for consistency in defining antecedent basis. Other more substantive amendments are discussed herein. No new matter has been added. The rejections of claims 30, 32-34, 40-45 and 50-52 under 35 U.S.C. §103(a) and non-statutory double patenting have been withdrawn. However, the Examiner has asserted new grounds of rejection, which are addressed herein.

Rejection under 35 U.S.C. §102(b)

In the Office Action, claim 30 is presumably rejected under 35 U.S.C. §102(b) as being anticipated by Hegel (U.S. Patent No. 5,255,157), which is directed to plastic pin grid array packages comprising a multilayer printed wiring board with an array of pins extending from one face thereof. Although the Examiner asserted that claim 30 is rejected under 35 U.S.C. §102(e), the text of §102(b) is quoted as forming the basis for the rejection under this section of the Office Action. Therefore, applicant assumes that the reference to §102(e) in paragraph 4 of the Office Action is a typographical error.

With respect to claim 30, the Examiner asserted that Hegel teaches providing a semiconductor chip 13 and a laminate 10 defining first and second major faces, wherein the laminate 10 includes an electrically conductive layer, and an underlying substrate (i.e., the multi-layer structure) supporting the electrically conductive layer (col. 2, lines 59-65; Fig. 4). The Examiner further asserted that Hegel teaches that at least one void 21 is in the laminate so as to extend from one of the major faces through the electrically conductive layer at least as far as the underlying substrate, and encapsulating the semiconductor chip 13 and the laminate 10 with an encapsulant 16 such that the encapsulant 16 extends into the void 21 to contact the underlying substrate 10 (col. 4, lines 1-26; Fig. 4).

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Claim 30 has been amended herein and now recites, *inter alia*, "forming at least one void in said laminate so as to extend from one of said major faces through said electrically conductive layer and **into said underlying substrate, but not as far as said second major face.**" Support for this change appears in Fig. 3 of the present application showing the formation of a void 50 in the laminate 30 that extends from one of the major faces (labeled as 31 in Fig. 2) through the electrically conductive layer 36 and into the underlying substrate 38, which void 50 is formed by the method of claim 30, as amended herein. Note that the void 50 does not extend as far as the second major face, which is identified as "32" in Fig. 2. Drawings alone may provide a "written description" of an invention as required by §112. *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1565, 19 USPQ2d 1111, 1118 (Fed. Cir. 1991). Moreover, the step of forming the void 50 in the laminate 30 so as to extend into the underlying substrate 38 is clearly supported in the specification of the present application on pages 7 and 10. Accordingly, no new matter has been added.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. There is nothing in the Hegel patent that expressly nor inherently suggests a method of encapsulating an integrated circuit comprising, *inter alia*, forming at least one void in the laminate so as to extend from one major face through the electrically conductive layer and into the underlying substrate, but not as far as the second major face. In fact, Hegel teaches away from the present application by noting throughout the specification, and illustrating in Fig. 4, that the multilayer printed wiring board 10 has a ring or array of holes 21 that pass or extend completely through the board 10 (see abstract; col. 2, line 17; col. 3, lines 67-68; col. 4, lines 1, 20-21 and 35-36; and Fig. 4). This is in direct contrast to the present invention that, as amended, defines forming at least one void 50 in the laminate 30 that extends into the underlying substrate 38, but not as far as the second major face (not completely through the laminate 30).

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Hegel does not teach or suggest forming at least one void on the laminate so as to extend from one major face through the electrically conductive layer and into the underlying substrate, but not as far as the second major face. Because in order to anticipate a claim the reference must teach every element thereof, Hegel cannot support the instant rejection of claim 30. Accordingly, applicant respectfully requests that the rejection by withdrawn.

Rejection under 35 U.S.C. §103(a)

Also in the Office Action, claims 32-44, 50 and 52 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hegel as applied above, and further in view of Juskey et al. (U.S. Patent No. 5,336,931). The Juskey patent is directed to a flow formed encapsulated integrated circuit package including a printed circuit substrate having upper and lower opposed surfaces and one or more anchor holes.

With respect to independent claims 32 and 40, in support of the instant rejection, the Examiner asserted that Hegel discloses a substrate 10 with a plurality of individual laminate layers, wherein all of the layers have a void (i.e., cavity) that is over the void of the plurality of layers, and the plurality of individual layers is over one another. A conductive layer is over the fourth laminate, so as to define a void portion over the void 21 portion of the fourth laminate layer (col. 2, lines 59-68; Fig. 4). Although Hegel fails to disclose forming a solder resist layer over the conductive layer, so as to define a void portion over the void portion of the conductive layer, the Examiner also asserted that Juskey et al. disclose forming a solder resist layer over the substrate 160, so as to define a void portion over the void portion. Thus, the solder resist when attached to the laminate of Hegel would be over the conductive layer, so as to define a void portion over the void portion of the conductive layer. The Examiner further asserted that it is well known in the semiconductor industry to have a substrate having at least one resin layer as evident by Juskey et al. (col. 3, lines 20-25). As such, the Examiner concluded it would have been obvious to incorporate the solder resist layer with the process of Hegel, since the solder resist would facilitate the formation of metal patterns on the

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laminate that are used as connection areas for bonding wires extending from the chip as taught by Juskey et al.

Claim 32 is amended herein and now defines a method of forming a laminate to lock an encapsulant comprising, *inter alia*, forming at least one continuous laminate layer; forming a second laminate layer over the continuous laminate layer, so as to define an underlying cavity; and forming a third laminate layer over the second laminate layer, so as to define a void portion over the underlying cavity. New claim 53 is added herein, which claim recites that the void extends into the laminate, but not entirely through the continuous laminate layer. Also, claim 40 is amended herein and now defines a method of encapsulating an integrated circuit comprising, *inter alia*, providing a substrate having at least one continuous laminate layer and at least one resin layer over the continuous laminate layer; and forming a void in the at least one resin layer and the at least one laminate layer such that a portion of the void located in the at least one resin layer is below a remaining portion of the at least one laminate layer, wherein the void does not extend through the continuous laminate layer. Support for these amendments appear in Figs. 3 and 4, which show the formation of at least one continuous laminate layer, and a void that does not extend through the continuous laminate layer. Because drawings alone may provide a "written description" of an invention as required by §112, no new matter has been added.

In order to "support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." MPEP 2142 (citing *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985)). For the following reasons, applicant submits that the Examiner has not met this burden and respectfully requests that the rejection be withdrawn.

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In order to establish a *prima facie* case of obviousness, *inter alia*, all of the claimed limitations must be taught or suggested by the prior art. MPEP 2143.03 (citing *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)). As noted herein, Hegel teaches that the multilayer printed wiring board 10 has a ring or array of holes 21 that pass or extend completely through the board 10 (*see* abstract; col. 2, line 17; col. 3, lines 67-68; col. 4, lines 1, 20-21 and 35-36; and Fig. 4). In contrast, independent claims 32 and 40 (as amended herein) define forming at least one continuous laminate layer and a void that does not extend through the continuous laminate layer. As such, the continuous laminate layer remains "continuous" after forming the void. Given that Hegel teaches holes that pass or extend completely through the board, this reference cannot teach or suggest forming or otherwise providing at least one continuous laminate layer, nor forming a void that does not extend through the continuous laminate layer.

Moreover, Juskey et al. do not fulfill the deficiencies of Hegel, as Juskey et al. teach that the upper solder mask 180 does not cover the anchor hole 150, whereas the lower solder mask 190 does cover the anchor hole 150. The lower solder mask 190 thereby acts as a bottom to the anchor hole 150 to prevent the cover forming material from flowing out through the bottom of the anchor hole 150 during the flow forming of the cover 110 (*see* col. 4, lines 1-9; and Fig. 2). As such, Juskey et al. do not teach or suggest forming at least one continuous laminate layer, nor forming a void that does not extend through the continuous laminate layer. If Juskey et al. had taught such a method, the lower solder mask 190 would not have been employed to prevent the cover forming material from flowing out of the anchor hole 150.

Neither Hegel nor Juskey et al. can be relied upon in support of the rejection of independent claims 32 and 40, as neither reference teaches or suggests all of the claimed limitations. Also, claims 33-34, 41-45 and 50-52 contain all of the limitations of the base claim from which they depend. While U.S. Patent Nos. 5,623,006 to Papathomas and 5,355,283 to Marrs et al. are cited in support of the rejection of claims 45 and 51, as noted above, these claims contain all of the limitations of the base claim

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from which they depend. Accordingly, for all of the reasons set forth above, applicant submits that the Examiner has not presented a *prima facie* case of obviousness and respectfully requests that the rejection be withdrawn.

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Conclusion

Applicant respectfully submits that, in view of the above amendments and remarks, the application is in condition for allowance. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,
DINSMORE & SHOHL LLP

By _____
Brian L. Smiler
Registration No. 46,458

One Dayton Centre
One South Main Street, Suite 500
Dayton, Ohio 45402-2023
Telephone: (937) 223-2050
Facsimile: (937) 223-0724
E-mail: brian.smiler@dinslaw.com
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